REMARKS

Claims 37-72 were previously pending in the application. Claims 68-72 are cancelled leaving claims 37-67 for consideration. Non-elected claims 68-72 may of course be made the subject of a divisional application to be filed at any time during the pendency of this application.

Claims 37-40, 41, 45 and 47 are rejected as unpatentable over LI et al. 5,623,387 in view of MAEDA 5,471,082. This rejection is respectfully traversed.

The position set forth in the Official Action is that LI et al. disclose most of the elements recited in claim 37 except for a vertical bipolar transistor. In an attempt to overcome this shortcoming, the Official Action offers MAEDA which teaches a vertical bipolar transistor. The reasons set forth in the Official Action for combining the two references is that both references are directed to solving the problem of ESD production and that MAEDA teaches that vertical bipolar transistors have an advantage over lateral bipolar transistors in their ability to conduct excessive currents.

The position set forth in the Official Action is untenable for at least the following reasons.

First, MPEP §2143.01 states that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render

the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

An object of LI et al. as set forth on column 6, lines 33-43 is to have a split bipolar transistor wherein the base contact is on an opposite side of the emitter from the base and at least twice as far from the base as is the emitter contact. This results in a significant resistance between a base contact and the base. Higher base resistance allows the transistor to turn on and respond to a low voltage, and the base contact is not in danger of overheating during an ESD event since maximum heat is generated in the base region itself, particularly at the base collector junction. As seen in Figure 5B of LI et al., base contact 314 is separated from emitter contact 309 by region 311. This allows the base contact 314 to be at least twice as far from the base (the region under field oxide 306b) as is the emitter contact 309.

As seen in Figure 38 of MAEDA, for example, the base region is denoted element 67a. Both the base contact b and the emitter contact e are the same distance from base 67a. Accordingly, incorporating the vertical bipolar transistor structure of MAEDA into the device of LI et al. would not allow the base contact to be at least twice as far from the base as the emitter contact. Such proposed modification would change the principle of operation of LI et al. and thus the teachings of the

references are not sufficient to render claim 37 of the present invention *prima facie* obvious.

In addition, MPEP §2141.02 states that a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 US 851 (1984).

Column 1, line 19 through column 3, line 26 of MAEDA disclose a horizontal type bipolar transistor similar to that of LI et al. The above passages of MAEDA teach the disadvantages of using horizontal type bipolar transistors. One of ordinary skill in the art would not look to the teachings of a horizontal bipolar transistor based on the teachings of MAEDA. Accordingly, one of ordinary skill in the art would not be motivated to combine the horizontal bipolar transistor teachings of LI et al. with MAEDA to render obvious the claims of the present invention.

Further, MPEP §2143.01 also provides that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Column 3, lines 15-35 of MAEDA, noted in the Official Action, teach the advantages and disadvantages of horizontal bipolar transistors and vertical bipolar transistors. Although

both devices are used as electrostatic discharge protection devices, the steps for manufacturing each of the different devices and the advantages provided by each of the devices are unique to the particular device chosen. Therefore, one of ordinary skill in the art would not be motivated to substitute a vertical bipolar transistor for a horizontal bipolar transistor or vice versa. There are many factors to take into account such that these transistors are not readily interchangeable.

For example, LI et al. at column 6, lines 1-11 teach that base-to-emitter resistors in the ESD protection devices are sized and shaped to have higher resistance than a base-to-emitter resistance of parasitic bipolar transistors. This sizing and shaping makes it easier for the ESD protection device to go into snap-back mode than the parasitic bipolar transistors. In contrast, column 11, lines 22-32 of MAEDA in conjunction with Figure 8, teach that the base-to-emitter must be shorted (see also claim 1 and claim 6 of MAEDA). Accordingly, the configuration of the MAEDA reference is completely different from the configuration taught by LI et al, which teaches having a higher base-to-emitter resistance of the ESD protection devices.

Therefore, there would be no desirability to combine the teachings of MAEDA with the teachings of LI et al. and thus the proposed combination suggested in the Official Action would not be obvious to one having ordinary skill in the art.

Accordingly, claim 37 is believed patentable over the proposed combination of references.

Claims 38-40, 41, 45 and 47 depend from claim 37 and further define the invention and are also believed patentable over the proposed combination of references.

In addition, claim 38 provides that a base and a collector of a vertical bipolar transistor are formed in a direction from a surface of the semiconductor substrate to a depth and an emitter of the vertical bipolar transistor is formed on the surface of the semiconductor substrate.

By way of example, Figure 3 of the present application shows base 16 and collector 17 of the vertical bipolar transistor of the ESD production element 210 are formed in a direction from a surface of the semiconductor substrate to a depth. Specifically, as seen in Figure 3 of the present invention, both the base 16 and collector 17 are buried within substrate 51. Emitter 11 is also buried within substrate 51 such that it is at the surface of substrate 51.

Figures 31-38 and the corresponding passages on column 14, line 43 through column 15, line 47 of MAEDA show collector 62 formed in substrate 61. However, thereafter epitaxial layer 64 is grown and base 67a is formed in the epitaxial layer. Emitter 80a is also formed in epitaxially grown layer 64. Accordingly, both the base 67a and emitter 80a of MAEDA are above the surface of substrate 61. MAEDA does not disclose or suggest that a base

and a collector are formed in a direction from a surface of the semiconductor substrate to a depth and an emitter of the vertical bipolar transistor is formed on the surface of the substrate as recited in claim 38 of the present invention.

As to claims 39, 40 and 41, LI et al. is offered for these teachings. However, as set forth above, LI et al. teach a horizontal bipolar transistor, not a vertical bipolar transistor. The Official Action cannot pick and choose certain elements from the horizontal bipolar transistor of LI et al. and combine them with the vertical bipolar transistor of MAEDA. As set forth above, manufacturing methods and resultant structure of the two types of transistors are not combinable. Either one or the other is chosen. Therefore, the proposed combination of references would not render obvious the features recited in the dependent claims.

Claims 42-44 are rejected as unpatentable over LI et al. in view of MAEDA and further in view of MCCLURE et al. 5,774,318. This rejection is respectfully traversed.

MCCLURE et al. is only cited for the teaching of forward diodes. MCCLURE et al. do not disclose or suggest what is recited in claim 37. As set forth above, LI et al. in view of MAEDA do not disclose or suggest what is recited in claim 37. Since claims 42-44 depend from claim 37 and further define the invention, the proposed combination of references would not render obvious claims 42-44. In addition, MCCLURE et al. teach a

horizontal bipolar transistor. Any teachings of MCCLURE et al. as to a horizontal bipolar transistor would be irrelevant to a vertical bipolar transistor as recited in the present invention.

Claims 49 and 51 are rejected as unpatentable over LI et al. in view of MAEDA and further in view of MCCLURE et al. This rejection is respectfully traversed.

As set forth above, since the teachings of MCCLURE et al. are with respect to a horizontal bipolar transistor, MCCLURE et al. would not be relevant to a vertical bipolar transistor. In addition, claims 49 and 51 depend from claim 37. As set forth above, the proposed combination of references does not teach or suggest what is recited in claim 37. Accordingly, the proposed combination of references would not render obvious claims 49 and 51.

Claims 46, 48, 50, 52 and 56 are rejected as unpatentable over LI et al. in view of MAEDA and further in view of A. SEDRA et al., textbook, Microelectronic Circuits. This rejection is respectfully traversed.

A. SEDRA et al. is only cited for the teaching that NPN transistors and PNP transistors are functionally equivalent. A. SEDRA et al. do not teach or suggest what is recited in claim 37. As set forth above, LI et al. in view of MAEDA do not teach or suggest what is recited in claim 37. Since claims 46, 48, 50, 52 and 56 depend from claim 37 and further define the invention, the proposed combination of references would not render obvious

claims 46, 48, 50, 52 and 56. In addition, A. SEDRA et al. is directed to a horizontal bipolar transistor. As set forth above, the teachings of a horizontal bipolar transistor would not apply to a vertical bipolar transistor. Accordingly, A. SEDRA et al. with LI et al. and MAEDA would not render obvious claims 46, 48, 50, 52 and 56.

Claims 53 and 54 are rejected as unpatentable over LI et al. in view of MAEDA and further in view of SHIGEHARA et al. 5,539,327 and KINUSAGA et al. 5,821,797. This rejection is respectfully traversed.

SHIGEHARA et al. and KINUSAGA et al. are only cited for the teaching of specific connections of a pad and of a bipolar transistor. SHIGEHARA et al. and KINUSAGA et al. do not disclose or suggest what is recited in claim 37. As set forth above, LI et al. in view of MAEDA do not disclose or suggest what is recited in claim 37. Since claims 53 and 54 depend from claim 37 and further define the invention, the proposed combination of references would not render obvious claims 53 and 54. In addition, both SHIGEHARA et al. and KINUSAGA et al. are directed to horizontal bipolar transistors. As set forth above, one of ordinary skill in the art would not use the teachings of horizontal bipolar transistors to render obvious the vertical bipolar transistors as recited in claims 53 and 54 of the present invention.

Claim 55 is rejected as unpatentable over LI et al. in view of MAEDA, SHIGEHARA et al. and KINUSAGA et al. and further in view of A. SEDRA et al. This rejection is respectfully traversed.

As set forth above, none of the proposed combinations of references teach or suggest what is recited in claim 37. Since claim 55 depends from claim 37 and further defines the invention, the proposed combination of references would not render obvious claim 55.

As to claims 57-67, these claims also depend from claim 37 and further define the invention. As set forth above, none of the proposed combinations of references teach or suggest what is recited in claim 37. Accordingly, claims 57-67 are also believed patentable over the cited prior art.

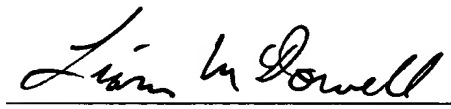
In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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